UNITED STATES PATENT APPLICATION FOR:

CHIP-JOIN PROCESS TO REDUCE ELONGATION MISMATCH BETWEEN THE ADHERENTS AND SEMICONDUCTOR PACKAGE MADE THEREBY

Inventor(s):

Biju CHANDRAN

Carlos A. GONZALEZ

Prepared by:

Antonelli, Terry, Stout & Kraus, LLP
1300 North Seventeenth Street, Suite 1800
Arlington, Virginia 22209
Tel: 703/312-6600
Fax: 703/312-6666

CHIP-JOIN PROCESS TO REDUCE ELONGATION MISMATCH BETWEEN THE ADHERENTS AND SEMICONDUCTOR PACKAGE MADE THEREBY

Field

The invention relates to an electronic assembly and a method of making the same. More particularly, the invention relates to an improved method of soldering a semiconductor chip to a substrate and to the semiconductor package made thereby.

Background

A conventional semiconductor package 1 illustrated in Figures 7A and 7B includes a package substrate 2 and a semiconductor chip or die 3 located on the substrate. The lower or frontside of the chip carries an integrated circuit which has a plurality of sites or connections for purposes of electrically contacting the integrated circuit to respective contact pads 4 on the package substrate, electronically connecting the chip to the package substrate. More particularly, the die has standoffs 5 mounted thereon. The standoffs are formed of an electrically conductive, high melting temperature material, such as copper. The

standoffs are electrically connected to the respective sites or connections of the integrated circuit on the chip. Soldered joints 6 in turn join the die standoffs to the contact pads on the package substrate. The soldered joints are formed in the conventional assembly process wherein the die with standoffs and the substrate with contact pads to which solder has been previously applied, are located in contact with one another and heated together to a temperature higher than the solder melting temperature and allowed to cool-down together. The solder on the contact pads of the substrate is reflowed during this joining process to wet the standoffs and form the soldered joints.

The semiconductor chip in the conventional semiconductor package is typically made of silicon, which has a coefficient of thermal expansion (CTE) of about 2.6-3.3 ppm/°C (parts per million per °C). In the past, the package substrate was generally made of a ceramic material, which has a CTE that is typically below 6 ppm/°C. During heating or cooling of the semiconductor package, including that associated with soldering during assembly of the package, the mismatch of the CTEs of the semiconductor chip and the package substrate was not of a magnitude which caused substantial bending of the semiconductor chip. Nevertheless, this mismatch can still present problems, especially in brittle materials from residual stresses as a result of soldering.

In recent years, there has been a move away from the use of ceramic as a package substrate material to alternative materials, such as plastics or other organic materials, which have lower cost, superior electrical characteristics. A problem with these alternate materials is that they usually have relatively high CTEs, compared to the CTE of the semiconductor chip. Some plastic substrates, for example, have CTEs on the order of 17 ppm/°C. The relatively larger CTE mismatch in packages using the higher CTE package substrate materials can induce adverse effects such as solder fatigue, package and die warpage, die cracking, etc. These problems can occur at the time of joining the chip to the substrate or subsequently during the operating life of the package.

Numerous proposals have been made to reduce the problems arising from CTE mismatch in package materials. For example, U.S. Patent No. 5,369,551 proposes a surface mount stress relief interface system and method wherein a compliant interface device is connected to both the substrate and chip for obviating CTE mismatch. In Assignee's U.S. Patent No. 5,889,652, a bond portion of the substrate is separated from a contact portion of the substrate by a flexible portion to allow relative movement to minimize the stresses on the solder joints.

U.S. Patent No. 5,931,311 discloses a standoff controlled interconnection for use in a soldering process to reduce solder joint plastic deformation caused by CTE mismatch. The patentees explain that the larger the standoff, the less plastic deformation that occurs, thus leading to a longer component/interconnection durability and cycles life.

Another approach taken to reduce the effect of CTE mismatch on the life of the semiconductor package involves reinforcement of the chip against warpage. For example, the use of a protective layer on the backside of the die is suggested in Assignee's U.S. Patent No. 5,936,304. In a further example, the semiconductor chip is provided with beveled edges which, together with an epoxy located thereon, reduce stresses on the chip when the package is heated, as disclosed in Assignee's U.S. Patent No. 6,049,124.

The problems related to CTE mismatch induced effects on semiconductor packages have become more pronounced as dies have become larger because of the increased distance from the center of the die to sites at which the die and substrate are joined to one another. There is a need for an improved method of joining CTE mismatched materials and an electronic assembly/semiconductor

package made thereby, wherein CTE mismatch induced effects such as solder fatigue, package and die warpage, die cracking, etc., are reduced or minimized.

Brief Description of the Drawings

The file of this patent contains at least one drawing executed in color. Copies of this patent with color drawing(s) will be provided by the Patent and Trademark Office upon request and payment of the necessary fee.

Fig. 1 is a schematic, sectional view of the right half, from the center line CL, of an assembly of a die on a substrate.

Fig. 2 is a schematic representation of a method of an example embodiment of the present invention for making a semiconductor package according to the invention.

Figs. 3A-3C and 3D-3E are respectively color coded temperature distributions on a die and the substrate made according to the method of Fig. 2 at different times, e.g., wherein Figs. 3A-3C are for the time one second after the die is placed on the substrate, and Fig. 3A is a cross sectional view through a portion of the die and substrate assembly, Fig. 3B is a view of the right end of the substrate in Fig. 3A and Fig. 3C is an enlarged view of the joint area within box A in Fig. 3A, and wherein Figs. 3D-3E are for the time 10 minutes into cooling

and Fig. 3D is a cross sectional view through a portion of the assembly and Fig. 3E is an end view of the right side of the substrate shown in Fig. 3D.

Fig. 4 is a graph of temperature versus time at representative regions of the package during the method of the invention as derived from a simulation using a transient thermal model of the example embodiment.

Fig. 5 is a graph of stress and warpage for the semiconductor package of the example embodiment obtained by simulation using the transient thermal model compared with those for the same package made using the conventional process.

Fig. 6 is a graph of the surface warpage, obtained by simulation using the transient thermal model, versus distance along the die from the center of the die for the example embodiment compared with the warpage for the same package made using the conventional method.

Fig. 7A is a schematic, cross sectional view through the right half, from the center line CL to the right, of a conventional package.

Fig. 7B is an enlarged view of the portion of the semiconductor package of Fig. 7A within the box B in Fig. 7A.

Detailed Description

The improved method of the invention of joining first and second CTE mismatched members to one another addresses the aforementioned need by reducing the elongation mismatch produced during cool-down after joining the members at an elevated temperature, by soldering in the example embodiment. Unlike the conventional method described above with reference to Figures 7A and 7B, wherein during soldering the members are heated together to a temperature higher than the solder melting temperature and allowed to cool-down together, the present invention is based upon the principle that when two adherents are attached at higher temperature, if they have the same elongation at the temperature at which the adhesive/solder solidifies, both adherents will contract the same amount and, hence, no stresses will be induced. For CTE matched adherents, the condition that the elongation of the adherents be equal will be true at any temperature. For CTE mismatched adherents, the adherents will have to be at different temperatures for this condition to hold. The method of the present invention exploits this principle by thermally expanding each of CTE mismatched members substantially the same amount in a direction along surfaces thereof to be joined at an elevated temperature, and thereafter joining the thermally expanded members to one another.

In the example embodiment as depicted in Figs. 1-3E, the two members are a semiconductor chip 7 and a substrate 8 which are joined to one another by soldering to form a semiconductor package 9. The die and substrate are at different uniform temperatures at the instant they are brought together for soldering. They are then allowed to cool-down together to room temperature. The temperatures of the die and the substrate are calculated so that their thermal expansions or elongations are substantially the same at the temperature the solder solidifies.

The technical basis underlying the present invention is explained with reference to Figure 1 wherein the chip or die 7 is joined to the substrate 8 by a plurality of soldered joints 10. The CTEs of the die, α_{die} and the substrate, α_{sub}, are different, e.g., in the example embodiment the difference between the CTEs is greater than 2.7 ppm/°C. More particularly, in the example embodiment it is assumed α_{die} is 2.6 ppm/°C and α_{sub} is 16 ppm/°C. The temperatures of the die and substrate at the instant the die is coupled to the substrate (when the melting solder is on the die, $T_{die}=T_{melting}$ of solder) are denoted by T_{die} and T_{sub}, respectively. The parameter L in Fig. 1 is the half length of the die (or more precisely the distance from the center of the die to the outermost bump or soldered joint 10). At the solder solidification temperature (or solder melting

temperature in the case of eutectic solders), the elongation of the die, Δl_{die}, and that of the substrate, Δl_{sub} (at the region of the outermost soldered joint 10), are expressed by:

(1) $\Delta l_{die} = \alpha_{die} (T_{die} - T_{room})L$

(2) $\Delta l_{sub} = \alpha_{sub} (T_{sub} - T_{room})L$

If Δl_{die} and Δl_{sub} are equal, then, when the soldered assembly cools down to room temperature, the die and the substrate would have contracted as much as they expanded (almost), and there will be no CTE mismatch induced effects (ideal case) from the joining method.

For that to happen,

(3) $\Delta l_{die} = \Delta l_{sub} = \alpha_{die} (T_{die} - T_{Room})L = \alpha_{sub} (T_{sub} - T_{Room})L$, i.e.,

(4) $$\frac{T_{die}^{aboveroom}}{T_{sub}^{aboveroom}} = \frac{\alpha_{sub}}{\alpha_{die}} = \frac{16ppm/°C}{2.6ppm/°C} = 6.15$$

Considering the example case of the package 9 being soldered with a eutectic AgSn solder which has a melting point of 221°C wherein the solder is on the die side before joining, and a copper bump or standoff 11 is on the substrate side, the temperature of the die for soldering T_{die} has to be at least 221°C. Assuming that T_{die} is selected to be 240°C in the joining method according to the invention, then

the substrate temperature T_{sub} has to be 57.4°C for the die and substrate to be thermally expanded substantially the same amount in a direction along the surfaces thereof to be joined by soldered joints 10.

The method of the example embodiment of the invention is illustrated in Fig. 2, wherein, as depicted in the left hand drawing of Figure 2, the die 7 and substrate 8 are separately heated by respective heat sources 11 and 12. In particular, the die with eutectic AgSn solder at the connection sites thereon is heated by heat source 11 to 240°C and the substrate 8 is heated by heat source 12 to 57.4°C so that they are each thermally expanded substantially the same amount. These temperatures are a function of the soldering temperature and the ratio of the coefficients of thermal expansion of $\alpha_{sub}/\ \alpha_{die}$, which ratio is 6.15 in the example. After the die and substrate are uniformly heated to their respective temperatures, they are aligned and the die is placed on the substrate as shown schematically in the center drawing in Figure 2. The soldered joints 10 are formed between the die and substrate upon assembly because the molten solder on the die wets the surfaces of the copper bumps on the substrate and is then solidified. The joined assembly is then cooled to room temperature, denoted by the right hand drawing in Figure 2.

Figures 3A-3E show temperature distribution in a transient thermal model of the example embodiment. At time zero in the method of the invention, the die and the AgSn solder thereon are at 240°C, and the substrate and substrate standoffs or bumps thereon are at 57.4°C. In this example, the assembly process (the time the die is on the substrate before cooling is allowed to begin) is assumed to take place for 10 seconds. During this time, heat conduction through the substrate bumps takes place and local regions of the substrate near the bumps get heated up (changing the condition from ideal). The longer the time the die is kept on the substrate before cooling is allowed to begin (this roughly translates to the time heat is applied to the die before it is removed), the case will deviate more from optimal. Following the assembly process, the die and the package are allowed to cool to room temperature in air. Figures 3A-3E show the temperature distribution in the package at different times in the assembly step and cooling step, namely one second after the die is placed on the substrate, Figures 3A-3C, and 10 minutes into cooling, Figures 3D and 3E.

Figure 4 graphically depicts the temperature distribution in representative regions of the package 9 during cooling. At the instant the solder temperature cools below 221°C (the melting/solidous temperature), relative motion is prevented between the die and the substrate and they form an assembly. It is

noted that in this example, which deviates from the ideal, the temperature in the die and the substrate at every instant in the cooling step is not such that their Δl's are the same. This means that there is some residual plastic deformation being built up in the soldered joints during cooling, changing the case from optimal. A cooling scheme can potentially be derived to reduce this deviation from the optimal condition. In any event, for the example embodiment, it is emphasized that the stress and warpage associated with the semiconductor package of the present invention after cooling it to room temperature are substantially reduced in comparison with those for the same case if the die and substrate were attached using the conventional process. This can be seen from a consideration of Figure 5.

Figure 5 compares the stresses in critical regions and die surface warpage for the example embodiment assembled using the described assembly method of the invention, and for the assembly of the same components joined by the conventional reflow process. Results indicate a significant improvement with the package of the invention as stresses and warpage as well as the normal force on the bump are reduced to less than one-half that in the package made by the conventional method wherein the substrate and semiconductor chip are cooled together from the solder solidification temperature to room temperature following

soldering of the soldered joints. The magnitude of the stresses and the warpage for the semiconductor package made according to the method of the present invention can be further decreased by reducing the time the assembly process takes (the time the die is heated after it is placed on the substrate). This time will correspond to the time the hot chuck, 11 in Figure 2, is in contact with the die after it has been placed on the substrate, and the temperature above solder melting temperature to which the die and solder thereon are heated.

Figure 6 illustrates the die surface warpage as a function of distance along the die from the center of the die to the soldered joint for the package of the example embodiment compared with the warpage for the same package made using the conventional process as referred to herein. It is seen that the warpage is less with the semiconductor package of the present invention as compared with that prepared by the conventional reflow die-attach process. In each case, warpage is seen to increase as a function of the distance from the center of the die. This evidences the fact that by means of the method of the present invention, the warpage experienced with large dies (such as those having a width of 200 mm, for example, where soldered joints are a considerable distance from the die center) can be reduced substantially when made by the method of the present invention.

This concludes the description of the example embodiment. Although the present invention has been described with reference to one illustrative embodiment thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this invention. For example, the thermal expansion before soldering is the same for the chip and substrate in the example embodiment but significant benefit can be obtained if the expansions are not identical but at least substantially the same, e.g., with ± 25% of one another or not differing by more than 2 ppm/°C. More particularly, reasonable variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the foregoing disclosure, the drawings and the appended claims without departing from the spirit of the invention. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.